	Search Text
1	S1 and S10
2	S1 and S12
3	creat$3 same customiz$3 same (book$1 or card$1 or image$1) and (plac$3 with order$1)
4	S1 and S8
5	creat$3 same customiz$3 same (book$1 or ((greeting$1 or post) adj1 card$1)) same order$3
6	creat$3 same customiz$3 same (book$1 or card$1) same credit$1
7	S1 and S6
8	creat$3 same customiz$3 same (book$1 or card$1) same order$3
9	715/765 or 345/619.ccls.
10	creat$3 same customiz$3 same (book$1 or card$1 or image$1) same credit$1
11	S1 and S4
12	creat$3 customiz$3 same (book$1 or ((greeting$1 or post) adj1 card$1)) same order$3
13	S1 and S2
14	S15 and S16
15	715/765 or 345/619.ccls.
16	plac$3 with order$4 with imag$3 with product$1
17	"20030222889"

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ERROR-CORRECTION CODE

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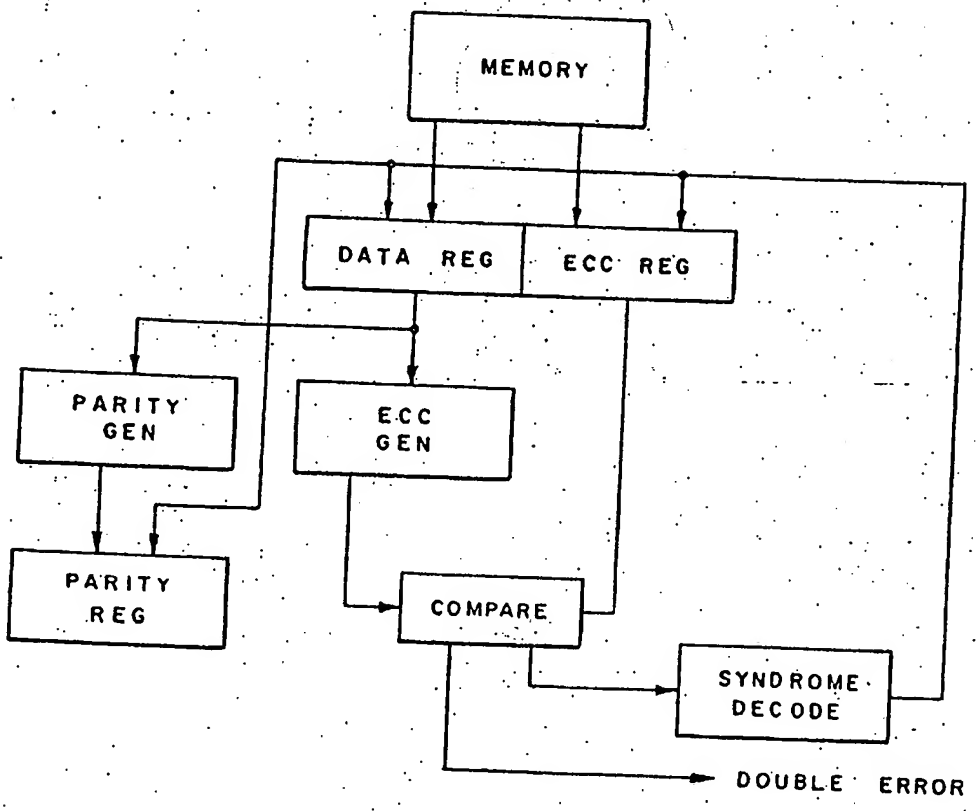

This memory stores data in an error-correcting code ECC that corrects single errors and detects double errors. In the memory a 72-bit word is made up of 64 data bits and 8 ECC bits. In the system associated with the memory, the 72-bit word of the memory is handled as 8 bytes each having 8 data bits and 1 parity bit.

During a read operation, the 64 data bits and the 8 ECC bits of the addressed word are stored in a register. The 64 data bits are supplied to a parity generator that generates the parity bits for the system associated with the memory. The 64 data bits are also supplied to an ECC generator that generates 8 ECC bits. A comparator receives the ECC bits from the register and from the generator and produces 8 syndrome bits. The latter signify a match or mismatch between the ECC bits stored

in the memory and the ECC bits generated from the data stored in the memory. A match signifies that there is no single or double error and the 64 data bits and the 8 parity bits are made available to the associated system. The 72-bit word of the register is then regenerated in the memory.

Three of the ECC bits form parity checks on the data and ECC bits in a pattern such that a mismatch identifies the byte in which the error occurs. Four of the ECC bits form parity checks in a pattern such that a mismatch identifies the bit position of the error within the identified byte. One ECC bit represents the parity of all 72 bits and thus distinguishes between single and double errors.

When a mismatch occurs during a read operation, the syndromes are decoded to locate the error and the appropriate stage of the register is triggered to correct the error. One stage of the parity register is also triggered at the byte location of the error. In a store operation, the word to be stored is checked for correct parity and 8 ECC bits are generated from the 64 data bits. The data and ECC bits are stored in the memory.

In a partial store operation, data is written into selected byte positions of a word and the data in the other byte positions is regenerated in the memory. The partial store operation is similar to either the read operation with error-correction followed by the store operation or to the generation of new ECC bits. However, if an error is found in the portion of the word that is not to be regenerated, the error-correction routine is not used.